



ST. ANNE'S

COLLEGE OF ENGINEERING AND TECHNOLOGY

(Approved by AICTE, New Delhi. Affiliated to Anna University, Chennai)
(An ISO 9001: 2015 Certified Institution)
ANGUCHETTYPALAYAM, PANRUTI – 607 106.

QUESTION BANK

JULY 2020 - NOV 2020 / ODD SEMESTER

BRANCH: CSE

YR/SEM: II/III

BATCH: 2019 – 2023

SUB CODE/NAME: CS8351–DIGITAL PRINCIPLES AND SYSTEM DESIGN

UNIT I

BOOLEAN ALGEBRA AND LOGIC GATES

PART A

1. Represent 3856 in BCD and 2421 code. (A/M 2019)
2. Simplify the following Boolean function. (A/M 2019)
$$F = x'y' + xy + x'y$$
3. State the classification of binary codes. (N/D 2018)
4. Define associative law. (N/D 2018)
5. Convert $(101101.1101)_2$ to decimal and hexadecimal form. (MJ 2013)
6. What are the limitations of karnaugh map? (MJ 2013 & (ND 2017-R2013)
7. Find the octal equivalent of hexadecimal numbers of AB.CD. (MJ 2014-R2013)
8. State and prove the consensus theorem. (MJ 2014-R2013, MJ 2017-R2013 & ND 2016-R2013)
9. Convert $(231.3)_{10}$ to binary. (MJ 2014-R2008)
10. Convert the binary number 10111011 into gray code. (MJ 2015-R2008)
11. What is mean by duality in Boolean algebra? (MJ 2015-R2008)
12. Convert $(0.6875)_{10}$ to binary. (MJ 2015-R2013)
13. Prove the following using DeMorgan's Theorem. $[(x+y)' + (x+y)']' = x+y$. (MJ 2015-R2013)
14. Find the octal equivalent of hexadecimal numbers of DC.BA. (MJ 2016-R2013)
15. What is meant by multilevel gates network? (MJ 2016-R2013)
16. Classify the logic families by its operations. (MJ 2017-R2013)
17. Write the truth table of AND and XOR gates. (ND 2010-R2008)
18. Perform the following code conversions: (ND 2011-R2008)
 $(1010.10)_{16} \rightarrow (?)_2 \rightarrow (?)_8 \rightarrow (?)_{10}$.
19. Convert $(1001010.1101001)_2$ to base 16 and $(231.07)_8$ to base 10. (ND 2013-R2008)
20. State the principle of duality. (ND 2014-R2013 & ND 2016-R2013)
21. Implement AND gate using only NOR gates. (ND 2014-R2013)
22. What is meant by self complementing code? (ND 2017-R2013)
23. Convert $(126)_{10}$ to Octal number and binary number. (ND 2015-R2013)

24. Write short notes on weighted binary codes. (ND 2015-R2013)
25. What is the difference between canonical and standard form?(ND 2019)
26. Given two binary numbers $A=1010010$ and $B=1000011$, find $A-B$ and $B-A$ using 2's complement?(ND 2019)

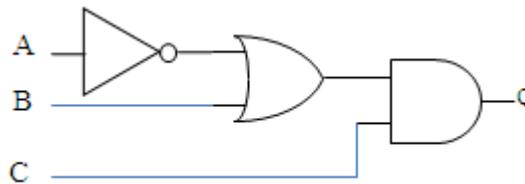
PART-B

NUMBER SYSTEMS

1. Convert the following numbers to decimal $(11011.101)_2$, $(5432)_6$. (4) (April/May 2019)
2. Perform the following arithmetic operation using 2's complement arithmetic operation using 2's complement arithmetic. $(11011100)_2 - (10011011)_2$. (3) (April/May 2019)
3. Add, subtract and multiply the following numbers in binary 110010 and 11101 .(6) (MJ 2014-R2008)
4. Convert $(1947)_{10}$ into its equivalent octal and decimal representation (10) (ND 2010-R2008)
5. Perform $(147-89)$ using 2's complement binary arithmetic. (6) (ND 2010-R2008)
6. Convert $(78.5)_{10}$ into binary.(3) (ND 2013-R2008).

LOGIC GATES

7. Convert the following logic system into NAND gates only.(8) MJ 2015-R2013)



8. Simplify the following expressions and implement them with two level NAND gate circuits: (16) (ND 2017-R2013)
 - i. $AB' + ABD + ABD' + A'C'D' + A'BC'$
 - ii. $BD + BCD' + AB'C'D'$
9. Implement the switching function $f(x,y,z) = \sum m(0,1,3,4,12,14,15)$ with NAND gates.(8) (ND 2016-R2013)

BOOLEAN EXPRESSION

10. Express the following functions in sum of minterms and product of maxterms. (6) (A/M'19)

$$F(ABCD) = A'B + BD + AC'$$
11. Demonstrate by means of truth tables the validity of the DeMorgan's theorem for three variables: (4) (A/M'19)

$$(XYZ)' = X' + Y' + Z'$$
12. Simplify the following Boolean function by means of a 4-variable map $F(A,B,C,D) = \sum m(0,2,4,5,8,10,14,15)$. (5) (A/M 2019)
13. Implement the following Boolean function only with NAND gates using a minimum number of gates inputs: $F(A,B,C,D) = AB + CD$. (4) (A/M'19)

14. Write short notes on Demorgan's theorem, Absorption law and consensus law. (13) (N/D 18)

15. Convert the following Boolean expression into standard SOP form: (6) (N/D 18)

$$AB'C + A'B' + ABC'D$$

16. Express the Boolean function $F = A + B'C$ in a sum of minterms (SOP). (7) (N/D 19)

17. Simplify the following expressions in (1) sum of the products and (2) products of sums : i)

$$x'z' + y'z' + yz' + xy$$

ii) $AC' + B'D + A'CD + A'BCD$

iii) $(A' + B' + D')(A + B' + C')(A' + B + D')(B + C' + D')$ (16) (ND 2017-R2013)

18. Simplify the following Boolean function in Sum of Products (SOP) and (Product of Sums (POS) $F(A,B,C,D) = \sum m(0,1,2,5,8,9,10)$. (10) (ND 2014-R2013).

19. Express the following function in sum of min-terms and product of max-terms

$$F(x,y,z) = x + yz. (8) (MJ 2015-R2013)$$

20. State and prove De Morgan's theorems (6/8) (ND 2010-R2008 & ND 2016-R2013)

21. Simplify the following expressions (i) SOP form (ii) POS form and implement functions using AND OR gates $F(A,B,C,D) = \sum m(0,1,2,5,8,9,10)$

KARNAUGH MAP METHOD

22. Reduce the following function using Karnaugh map technique: (16) (MJ 2013)

i) $f(A,B,C) = \sum m(0,1,3,7) + \sum d(2,5)$

ii) $F(w,x,y,z) = \sum m(0,7,8,9,10,12) + \sum d(2,5,13)$

23. Express the following function in a simplified manner using K map technique

24.

i. $G = \pi M(0,1,3,7,9,11)$.

ii. $f(W,X,Y,Z) = \sum m(0,7,8,9,10,12) + \sum d(2,5,13)$. (16) (MJ 2013)

25. Simplify the following Boolean expression in

(i) Sum of Product

(ii) Product of Sum using Karnaugh map.

$$AC' + B'D + A'CD + ABCD. (16) MJ 2015-R2013$$

26. Plot the following Boolean function in Karnaugh map and simplify it. $F(w,x,y,z) =$

$$\sum m(0,1,2,4,5,6,8,9,12,13,14). (6) (ND 2014-R2013).$$

27. Minimize the following expressions using K-Map

$$Y = A'BC'D' + A'BC'D + ABC'D' + A'B'CD'. (10) (ND 2016-R2013)$$

28. Simplify the following switching functions using Karnaugh map method and realize expression using gates $F(A,B,C,D) = \sum m(0,3,5,7,8,9,10,12,15)$. (16) (ND 2015-R2013).

29. What are Universal gates? Construct any four basic gates using only NAND and NOR gates.

QUINE MCCCLUSKEY OR TABULATION METHOD

30. Minimize the following expressions using Quine McClusky method.

$$Y = A'BC'D' + A'BC'D + ABC'D' + ABC'D + AB'C'D + A'B'CD'. (8) (ND 2016-R2013)$$

31. Simplify the function $F(w,x,y,z) = \sum m(2,3,12,13,14,15)$ using tabulation method. Implement the simplified function using gates. (16) (ND 2014-R2013).

32. Simplify the following switching functions using Quine McClusky's method and realize expression using gates $F(A,B,C,D) = \Sigma(0,5,7,8,9,10,11,14,15)$. (16) (ND 2015-R2013).
33. Simplify the following expression:

$$y = m_1 + m_3 + m_4 + m_7 + m_8 + m_9 + m_{10} + m_{11} + m_{12} + m_{14} \text{ using}$$

(i) Karnaugh Map

(ii) Quine McClusky method. (16) (MJ 2017-R2013)

UNIT –II

COMBINATIONAL LOGIC

PART-A

1. Construct a full adder using two half adders and OR gate. (April/May 2019)
2. Write the truth of 2 to 4 line decoder and draw its logic diagram. (A/M 2019).
3. Draw 1:8 Demultiplexer using two 1:4 Demultiplexers. (N/D 2018)
4. What is propagation delay? (N/D 2018)
5. Write down the truth table of a full subtractor. (MJ 2013-R2008 & ND 2017-R2013)
6. What is meant by Test Bench? (MJ 2013-R20)
7. Implement the function $G = \Sigma m(0,3)$ using a 2x 4 decoder. (MJ 2014-R2013)
8. Draw the circuit for 2 to 1 line multiplexer. (MJ 2014, ND 2016 & MJ 2017-R2013)
9. Realize $G = AB'C + DE + F'$ using NAND gates. (MJ 2014-R2008)
10. Realise 4 bit binary to gray code converter using EX-OR gates. (MJ 2014-R2008)
11. Give the truth table for a half adder and write the expression for sum and carry. (MJ 2015-R2008)
12. Write any two advantages of HDL. (MJ 2015-R2008)
13. Implement a full adder with 4x1 Multiplexer. (MJ 2015-R2013)
14. Write the Data flow description of a 4-bit Comparator. (MJ 2015-R2013)
15. Define Combinational Circuits. (MJ 2016-R2013)
16. Design the combinational circuit with 3 inputs and 1 output. The output is 1 when the binary value of the inputs is less than 3. The output is 0 otherwise. (MJ 2016-R2013)
17. What is priority encoder. (MJ 2017 & ND 2016 - R2013)
18. With block diagram show how a full adder can be designed by using two half adders and one OR gate. (ND 2011-R2008)
19. Obtain the truth table for BCD to Excess-3 code converter. (ND 2013-R2008)
20. Define a code converter logic circuit. (ND 2014-R2008)
21. What is half adder? Write its truth table. (ND 2014-R2008 & ND 2015-R2013)
22. Implement the following Boolean function using 8:1 multiplexer $F(A,B,C) = \Sigma m(1,3,5,6)$. (ND 2014-R2013)
23. What are binary decoders. (ND 2017-R2013)
24. Discuss NOR operation with truth table. (ND 2015-R2013)
25. What is multiplexer? Show the block diagram of 4x1 mux? (ND 2019)
26. What is magnitude comparator? (ND 2019)

PART – B

COMBINATIONAL LOGIC CIRCUITS

1. Design a 4 bit binary adder – subtractor circuit. (5) (A/M 2019)(ND 2019)
2. Design a full adder With inputs x, y, z and two outputs S and C . The circuit performs $x+y+z$, z is the input carry, C is the output carry and S is the Sum. (8) (MJ 2016-R2013)
3. Design a full subtractor with three inputs x and y and B_{in} and two outputs $Diff$ and B_{out} . The circuit subtracts the bits $x-y-B_{in}$ where B_{in} is the input borrow and $diff$ is the difference. OR Design a full subtractor and derive expression for difference and borrow. Realize using gates. (8) (ND 2015-R2013)
4. Design a logic circuit that accepts a 4 bit gray code and converts it into 4 bit binary code. (8) (MJ 2016-R2013)
5. Design a code converter that converts a binary to BCD code. (8) (ND 2015-R2013)
6. Design a combinational circuit that converts 8421 BCD code to Excess-3 code. (8) (ND 2016 & MJ 2014-R2013)
7. Design and implement binary to gray code convertor. (8) (ND 2017-R2013) & (ND 2014-R2008) *or* Design a combinational circuit to convert binary to gray code. (8) (MJ 2013-R2008 & ND 2016-R2013)
8. Design and implement a 8421 code to gray code convertor. Realize the converter using only NAND gates. (8) (ND 2014-R2013)
9. Compare and contrast between encoder and multiplexer. (8) (ND 2016-R2013)
10. What is BCD adder? Design an adder to perform arithmetic addition of two decimal digits in BCD. (ND 2019)

ENCODERS & DECODERS

11. Explain the logic diagram of a 4-input priority encoder. (8) (A/M 2019)
12. Explain in detail about encoders and decoders. (13) (N/D 2018)

MULTIPLEXERS

13. Design 32 to 1 Mux using four 8 to 1 Mux and 2 to 4 decoder. (13) (N/D 2018)
14. Implement the following Boolean function using 8 to 1 multiplexer and an inverter
 $F(A,B,C,D) = \sum m(2,4,6,9,10,11,15)$ (5) (A/M 2019)
15. Implement the following Boolean function using 8 to 1 multiplexer $F(A,B,C,D) = A'BD + ACD + B'CD + A'C'D$. Also implement the function using 16 to 1 multiplexer. (16) (MJ 2014-R2013)
16. Implement the switching function $F(A, B,C,D) = \sum m(0, 1, 3, 4,12,14,15)$ using 8 : 1 multiplexer. (8) (ND 2017-R2013)
17. Implement the Boolean function using 8:1 multiplexer $F(W,X,Y,Z)=W'XZ' + WYZ+ X'YZ+ W'Y'Z$. (16) (MJ 2017-R2013)

18. Implement the following boolean function with a multiplexer:

$$F(w,x,y,z) = \Sigma m(2,3,5,6,11,14,15). \text{ (8) (MJ 2015-R2013)}$$

19. Implement using Boolean function $F(X,Y,Z) = \Sigma(1,2,6,7)$ using multiplexer. (ND 2019)

HDL

19. Design a combinational circuit that accepts a 3 bit number and generates a 6 bit binary number output equal to the square of the input number. Write a high level behaviour description for the circuit. (8) (A/M 2019)

20. Construct a BCD adder circuit and write a HDL program module for the same. (8) (MJ 2017-R2013)

UNIT –III

SYNCHRONOUS SEQUENTIAL LOGIC

PART-A

1. State the difference between latches and flipflops. (A/M 2019)
2. What is meant by edge triggered flip flop? (A/M 2019, ND 2017 & MJ 2017)
3. State the operation of T flip flop (N/D 2018)
4. Mention the different types of shift registers? (N/D 2018)
5. How a synchronous counter differs from asynchronous counters? (ND 2017)
6. What is the operation of JK flip flop? (ND 2016)
7. Define race around condition. (ND 2016 & MJ 2017)
8. Write notes on propagation delay. (ND 2015)
9. Draw the diagram of T flip flop and discuss its working. (ND 2015)
10. With reference to a JK flip flop, what is racing? (ND 2014)
11. Distinguish Moore and Mealy circuit. (ND 2014)
12. State the excitation table of JK flip flop. (MJ 2016)
13. What is the minimum number of flip flops needed to build a counter of modulus 8. (MJ 2016)
14. What is ring counter? (MJ 2015)
15. Give the block diagram of Master Slave D flip flop. (MJ 2015)
16. Write the characteristic table and equation of JK flip flop. (MJ 2014)
17. Write any two applications of Shift register. (MJ 2014)
18. Define shift register. (AM 2015-R2008)
19. Write the characteristic equation of a JK flip flop. (AM 2015-R2008)
20. Write down the characteristic equation of SR flip flop.
21. State the rules for state assignment.
22. What is the minimum number of flip flops needed to design a counter of modulus 60?
23. Compare combinational and sequential circuits.
24. Why is the stimulus signal in a test bench synchronized to the inactive edge of clock of the sequential circuit that is to be tested? (ND 2019)

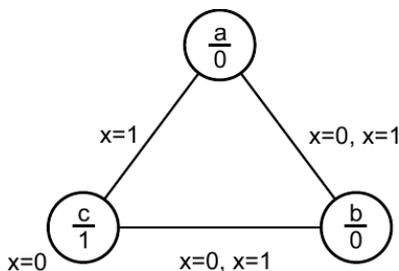
PART-B

SEQUENTIAL CIRCUITS-FLIP FLOPS

1. Explain the operation of JK FF,SR FF, T FF and D FF with a neat diagram. Also discuss their characteristic equation and excitation table. (13) (A/M 2019, ND 2017)
2. Construct a Clocked Master slave JK flip flop and explain. (5) (A/M 2019)
3. Design and implementation of SR flip flop using NOR gate (13) (N/D 2019)
4. Implement JK flip flop using D flip flop.(8) (ND 2016)
5. How race condition can be avoided in a flip flop.(8) (ND 2016&ND 2014)
6. Implement T flip flop and JK flip flop using D flip flop. (13) (MJ 2017) **OR**
Implement T flip flop using D flip flop and JK flip flop using D flip flop.(13) (MJ 2014)

ANALYSIS AND DESIGN OF CLOCKED SEQUENTIAL CIRCUITS

7. Design a sequential circuit with two D flip flop and B and one input X. When X=0, the state of the circuit remains the same. When X=1, the circuit goes through the state transitions from 00 to 10 to 11 to 01, back to 00 and then repeats. (8) (A/M 2019)
8. Realize the sequential circuit for the state diagram shown below.(8) (ND 2014)



9. A sequential circuit with two D flip flops A and B, two inputs x, and Y, and one output Z is specified by the following input equations: (8) (A/M 2019)

$$A(t+1) = x'y + xA$$

$$B(t+1) = x'B + xA$$

$$z = B$$

Draw the logic diagram of the circuit. Derive the state table and state diagram and state whether it is a Mealy or a Moore machine.

10. A sequential circuit with two D flip flops A and B, one input x, and one output z is specified by the following next state and output equations:

$$A(t+1) = A' + B,$$

$$B(t+1) = B'x$$

$$z = A + B'$$

- (i) Draw the logic diagram of the circuit.(4)
- (ii) Derive the state table.(3)
- (iii) Draw the state diagram of the circuit.(3) (MJ 2015)

11. Explain the differences between a state table, characteristic table and excitation table.(6) (MJ 2015)
12. Construct a 4 bit register using D-FF and explain the operations of the registers.(ND 2019)

COUNTERS

13. Explain in detail about 4 bit Johnson counter. (13) (N/D 2018)
14. Design Mod-7 counter using JK flip flop. (13) (ND 2017)
15. Design a MOD-10 synchronous counter using JK flip flops. Write execution table and state table.(13) (ND 2014)
16. Design and implement Mod-5 synchronous counter using JK flip flop and also draw the timing diagram.(13) (MJ 2017)
17. Design a modulo 5 synchronous counter using JK Flip Flop and implement it .Construct its timing diagram.(14) (MJ 2016)
18. Consider the design of 4-bit BCD counter that counts in the following way:
0000,0001,0010....,1001 and back to 0000.Draw the logic diagram of this circuit.(14) (ND 2016)
19. Design a three bit synchronous counter with T flip flop and draw the diagram.(13) (ND 2015)(ND 2019)
20. Design a binary counter using T flip flops to count in the following sequences: (14) (MJ 2016)
 - (i) 000,001,010,011,100,101,111,000
 - (ii) 000,100,111,010,011,000
21. Consider the design of a 4 bit BCD counter that counts in the following way:
0000,0001,0011....,1001 and back to 0000.
 - (i) Draw the state diagram.(4)
 - (ii) List the next state table.(4)
 - (iii) Draw the logic diagram of the circuit. (8) (MJ 2015)
22. Design a synchronous counter which counts in the sequence 000,001,010, 011,100,101, 110,111, 000 using D FF. (13) (MJ 2014)
23. Explain the operation of shift registers?(ND 2019)

UNIT- IV
ASYNCHRONOUS SEQUENTIAL LOGIC

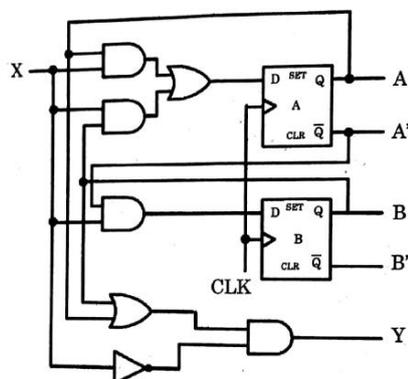
PART – A

1. Draw the logic diagram and write the function tables of D Latch. (A/M 19)
2. What is meant by race free condition in sequential circuits? (A/M 19)
3. Define race around condition. (N/D 2018, AM 2017)
4. Define the state table (N/D 2018)
5. What is asynchronous sequential circuit?
6. Define Merger graph. (ND 2017)
7. Define critical race and non critical race. (ND 2017 & MJ 2016)
8. What are races? (ND 2016)
9. Define flow table in asynchronous sequential circuits. (ND 2016)
10. What is race condition? (ND 2015 & MJ 2014)
11. Define Hazard. What are the causes of Hazards? (ND 2014) (ND 2019)
12. Draw the waveforms showing static 1 hazard. (MJ 2016)
13. Compare synchronous and asynchronous sequential circuit. (MJ 2015)
14. What are the types of hazards? (MJ 2014)
15. What happens when hazard happens in a logic circuit?
16. What is meant by essential hazards?
17. Draw the block diagram of an asynchronous sequential circuit.
18. Define static hazard and dynamic hazard.
19. What is primitive flow table?
20. What are static 1 and static 0 hazards?
21. Define fundamental mode circuit and pulse mode circuit.
22. Write down the steps involved in the design of synchronous sequential circuits.
23. What is a critical race condition? Give example.
24. Compare synchronous and asynchronous sequential circuit. (ND 2019)
25. What are hazard free digital circuits?
26. What are the types of asynchronous circuits?
27. Define flow table in asynchronous sequential circuit.
28. What is a critical race? Why should it be avoided?
29. What are the needs for asynchronous circuits? (ND 2019)

PART - B

1. Write the difference between synchronous and asynchronous sequential circuit. (4) (A/M 19)
2. Outline the procedure for analyzing asynchronous sequential circuit (9) (A/M 19) (ND 2019)

3. Discuss about the possible hazards and method to avoid them in combinational circuits, (5) (A/M 2019)
4. Discuss about the possible hazards in sequential circuits. (8) (A/M 2019)
5. Find the circuit that has no static hazards and implement the Boolean function $F(A,B,C,D) = \sum m(1,5,6,7)$ (13) (N/D 2018)
6. What are called as essential hazards? How does occur in sequential circuits? How can the same be eliminated using SR latches? Give an example. (13) (N/D 2018)
7. Explain about the designing of Asynchronous sequential circuits with example. (ND 2017)
OR Explain the steps for design of asynchronous sequential circuits. (ND 2016 & MJ 2014)
OR Summarize the design procedure of asynchronous sequential circuits. (AM 2017) (15)
8. What are Hazards and its types? How can you design a hazard free circuit, explain with example. (15)(ND 2017)
9. Explain the types of hazards in combinational circuits and sequential circuits and also demonstrate a hazard and its removal with example. (ND 2016& MJ 2015) OR Explain the types of hazards that occurs in asynchronous sequential circuits and combinational circuits. (AM 2017) (15)
10. Discuss in detail the procedure for reducing the flow table with an example. (MJ 2016) (13)
11. Design an asynchronous sequential circuit with 2 inputs X and Y and with one output Z wherever Y is 1, input X is transferred to Z. When Y is 0; the output does not change for ant change in X. Use SR latch for implementation of the circuit. (15) (MJ 2016) (15)
12. Explain the race free assignment procedure .(8) (MJ 2015) OR Explain race free state assignment with a an example.(13)
13. Implement the switching function $F = \sum m(1,3,6,7,8,9,14,15)$ by a static hazard free two level AND OR gate network. (15) (MJ 2014)
14. Analyze the following clocked sequential circuit and obtain the state equations and state diagram. (15) (ND 2015)



15. An asynchronous sequential circuit is described by $Y = X_1X_2' + (X_1 + X_2')Y$ AND $Z = Y$;
Draw the logic diagram and derive transition table and output map. (ND 2019)

UNIT – V

MEMORY AND PROGRAMMABLE LOGIC

PART-A

1. What is memory decoding? (MJ 2014, ND 2017 & MJ 2017)
2. What is programmable logic array? How it differs from ROM? (ND 2017)
3. List the differences between PLA and PAL. (MJ 2017)
4. How to detect double error and correct single error? (ND 2016 & AM 2015)
5. Give the comparison between EPROM and PLA. (ND 2016)
6. What is memory address register? (ND 2015)
7. Write short notes PLA. (ND 2015)
8. Whether PAL is same as PAL? Explain. (ND 2014)
9. What is volatile memory? Give example. (ND 2014)
10. Differentiate between EEPROM and PROM. (AM 2015)
11. Name the types of ROM. (AM 2011)
12. Compare and contrast static RAM and DRAM. (AM 2013) (ND 2019)
13. Determine the number of address lines required for 512 bytes of memory and for a 2kB memory. (AM 2011)
14. Define a memory cell. Give an example. (AM 2007)
15. What is access time of a memory?
16. Write a ASCII code for the decimal digit 9 with an even parity.
17. Determine the single error correcting code for the formation code 10111 for odd parity.
18. Implement the exclusive OR function using ROM.
19. What is memory cycle?
20. Compare the features of PROM, PAL and PLA.
21. How many 32KX8 RAM chips are needed to provide a memory capacity of 512KB?

PART-B

RAM & ROM

1. Give the internal block diagram of 4x4 RAM. (6)
2. Design a combinational circuit using ROM that accepts a three bit binary number and outputs a binary number equal to the square of the input number. (13)
3. Discuss on the concept of working and applications of semiconductor memories. (13)
4. Explain about the Random Access memory. (13)
5. What are the two types of Random Access memory? Explain them. (8)
6. What is ROM and why it is essential to use ROM in a computer? Explain types of ROM.

ERROR DETECTION AND CORRECTION

7. Explain about error detection and correction using hamming codes. (13) (ND 2017)
8. The following messages have been coded in the even parity hamming code and transmitted through a noisy channel. Decode the messages assuming that at most a single error has occurred in each code word. i) 1001001 ii) 0111001 iii) 1110110 iv) 0011011. (15)
9. Describe about the error detection code using parity bit. (8)

PLA & PAL

10. A combinational circuit is defined by the functions:

$$F_1 = \sum m(3,5,7), F_2 = \sum m(4,5,7).$$

Implement the circuit with a PLA having 3 inputs, 3 product terms and two outputs. (7)

11. Draw a PLA circuit to implement the logic functions: (5)

$$A'BC + AB'C + AC' \text{ and } A'B'C' + BC.$$

12. Implement the following using PLA. (13) (AM 2014)

$$A(x,y,z) = \sum m(1,2,4,6)$$

$$B(x,y,z) = \sum m(0,1,2,6,7)$$

$$C(x,y,z) = \sum m(2,6)$$

13. Draw a neat sketch showing implementation of

$$Z_1 = ab'd'e + a'b'c'd'e' + bc + de$$

$$Z_2 = a'c'e$$

$$Z_3 = bc + de + c'd'e' + bd \text{ and}$$

$$Z_4 = a'c'e + ce$$

using a 5x8x4 PLA. (13) (AM 2013)

14. Design a BCD to Excess-3 code converter and implement using suitable PLA. (13) (ND 2014)

15. Implement the following 2 Boolean functions with a PLA. (8) (AM 2015)(ND 2019)

$$F_1 = AB' + AC + A'BC'$$

$$F_2 = (AC + BC)'$$

16. Implement the following function using PAL. (13) (ND 2015)

$$F_1(A,B,C) = \sum (1,2,4,6)$$

$$F_2(A,B,C) = \sum (0,1,6,7)$$

$$F_3(A,B,C) = \sum (1,2,3,5,7).$$